Available online at www.sciencedirect.com

ScienceDirect

Procedia Engineering 00 (2011) 000–000

Procedia Engineering

www.elsevier.com/locate/procedia

Proc. Eurosensors XXV, September 4-7, 2011, Athens, Greece

An Enhanced, Highly Linear, Fully-Differential PLL-based Sensor Interface

Hans Danneels[a,*], Kristof Coddens[b], Georges Gielen[a]

[a]*K.U.Leuven, Dept. Elektrotechniek ESAT-MICAS, Leuven, Belgium*
[b]*Melexis, Tessenderlo, Belgium*

Abstract

Time-/frequency-to-digital conversion is gaining popularity since it benefits from the improved timing resolution in new technologies whereas voltage processing suffers from the reduced supply voltage. Due to their low-frequent nature, sensor signals specifically are interesting for such techniques since oversampling can be used to obtain the wanted accuracy. Frequency based conversion mechanisms however suffer from the non-linear conversion of the sensor signal into a frequency. Therefore, resolutions higher than 10-12 bit can only be obtained with proper calibration. This paper describes an enhanced differential PLL-based sensor interface architecture which overcomes this problem with linearity error down to 0.01% without calibration for a 0.35 um CMOS XFAB implementation.

Keywords: sensor interface; PLL-based conversion; Linear; oscillator-based; fully-differential;

1. Introduction

While digital logic is very suited for scaling and timing resolution improves in smaller technologies, analog circuits suffer more from disadvantages such as processing, environment-induced parameters and scaling supply voltage. Besides the issues of matching and noise, the threshold voltage (VT) is reduced less significant compared to the power supply. This results in a reduced signal range for analog signals in the voltage domain [1]. Traditional sensor interfaces transform the sensor signal into a voltage which is processed in the analog domain and digitized by an Analog-to-Digital Converter (ADC) as presented in Fig. 1A. Due to their analog nature, these interfaces are more sensitive to non-idealities. To make use of the time-benefits in smaller technologies, time based conversion methods are widely investigated [2]. These converters transform the wanted signal to time/frequency information by a Voltage-to-Time Converter. Thereafter, this information is digitized by a Time-to-Digital Converter (see Fig. 1B).

* Corresponding author. Tel.: +3216321888; fax: +3216321975.
E-mail address: hans.danneels@esat.kuleuven.be

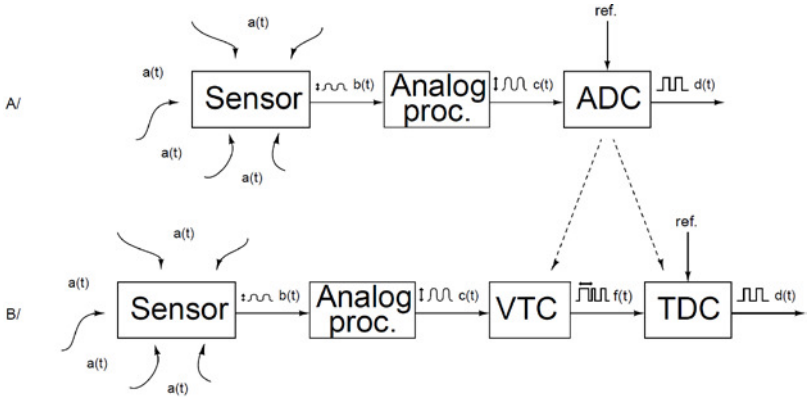

Fig. 1: Basic overview of a sensor interface system. On top (A) a conventional interface is demonstrated which processes the sensor signal in the analog voltage domain before quantizing the information. At the bottom (B) a schematic of an interface, based on time-information conversion mechanism is shown.

While suffering less from noise and scaling issues, the biggest disadvantage of time-based conversion is the non-linearity of the VTC. Traditionally, to overcome this non-linearity, power-hungry and expensive calibration steps are needed. This paper presents a fully-differential architecture which improves the linearity without these calibration steps.

2. The fully-differential PLL-based architecture

An example of a frequency based converter is given by [3,4]. This work demonstrates a highly digital PLL-based conversion mechanism where no external references are needed. Furthermore, noise shaping is performed without the need of a large analog loop filter. The single ended version (a) and differential schematic (b) of this converter are given by the two top schematics in figure 2.

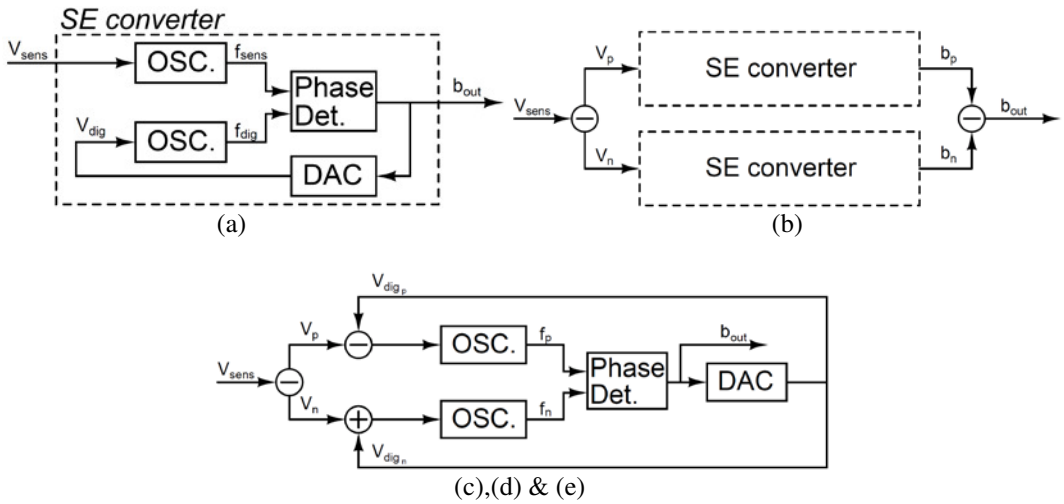

Fig. 2. *Overview of the different PLL-based architecture. The top schematic represents the (single bit) single ended architecture (a), the second schematic represents the original differential architecture (b), while the bottom schematic displays the new fully differential structure (c,d,e).*

This work presents an enhanced, fully-differential PLL-based architecture (see Fig. 2 bottom). In (a) en (b) the sensor signal steers one oscillator and the second oscillator tracks the sensor-dependant variation of the frequency f_{sens}. In (c), (d) and (e), however, the differential sensor signal steers both oscillators. This results in both oscillators drifting away in different directions from the quiescent frequency f_0 of the (matched) oscillators. The digital control signal pulls both oscillators back to f_0. A distinction is made between 3 versions which quantize the phase difference with 1-bit (c), 2-bit (d) or 3-bit (e) accuracy respectively.

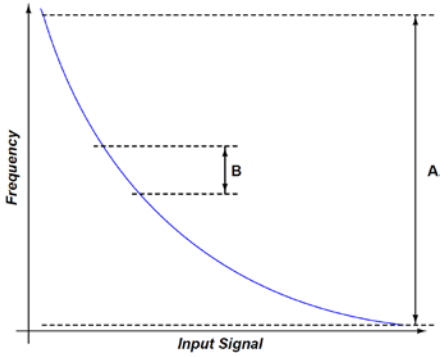

Fig 3. Schematic overview of the non-linear conversion of the input signal to the corresponding frequency. While in current frequency-based converters, the full range A is used, the proposed architecture reduces the range towards B by using feedback on 2 differentially steered oscillators without reducing the input signal range.

Figure 3 demonstrates the principle where the nonlinearity of the input signal towards the frequency is plotted for VCO-based VTCs. While (a) and (b) (and other VCO-based VTCs) use the full range A of the frequency span, the proposed architectures forces the frequency of the oscillators into the smaller span B around the quiescent frequency without reducing the dynamical range of the input signal. Increasing the number of bits reduces the frequency span B and improves the linearity.

3. Results

To prove the concept, Spectre simulations are done for XFAB 0.35u CMOS technology.

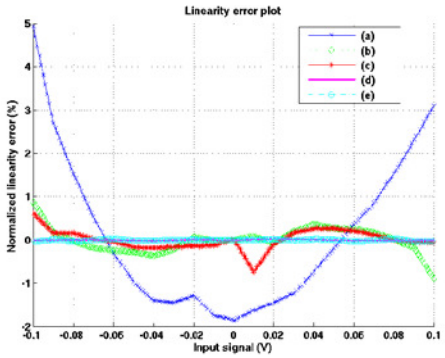

Fig 4. Normalized linearity error for the digital output signal of the 5 different architectures. The single-ended architecture (a) is highly nonlinear with errors up to 5%. The 2 and 3 bit architectures however accomplish a reduced linearity error of 0.03%.

The five different topologies are compared, with a VCO-implementation of a 5-stage coupled sawtooth oscillator [5] with f_0 going from 42 MHz to 53 MHz. The input sensor signal is derived from a bridge-configuration resistive pressure sensor with an input span of 200 mV and a conversion speed of 100 kHz is targeted for all the alternatives. Fig. 4 shows the normalized linearity of the digital output signal which is clearly much better for configurations (d) and (e). Table 1 depicts the performance where (a) consumes the least power but has a linearity error of 5%. Regarding linearity, (b) and (c) are comparable but (b) consumes much more power. When increasing the number of bits, the linearity further improves towards 0.01%. From 3 bits however, the power consumption increases due to the multi-bit overhead.

Table 1. Comparison of the different architectures.

Topology	***f_0 [MHz]***	***Power [mW]***	***Max Lin. Error [%]***	***Remarks***
Single ended (a) [3,4]	53	1.320	5	
Differential double (b) [3,4]	53	2.640	0.82	Double Power
Fully differential 1 bit (c) [this work]	53	1.980	0.61	Better Matching
Fully differential 2 bit (d) [this work]	***52.5***	***1.730***	***0.03***	***Better Matching***
Fully differential 3 bit (e) [this work]	***42***	***2.320***	***0.01***	***Better Matching***

Since the sensor is integrated in both oscillators of the proposed architectures, the matching of these oscillators is much better than for the work presented in [3,4]. Therefore, the influence of external factors (temperature, supply voltage,…) is reduced because their effect on the frequency is much more correlated for both oscillators and will therefore be cancelled out.

4. Conclusion

This paper presents a fully differential PLL-based sensor interface architecture which improves the linearity compared to current state-of-the-art alternatives with a factor of 82 to 500 without the addition of much power consumption. Transistor level simulations (Spectre) in XFAB 0.35 µm CMOS technology have been done to prove the feasibility of the system.

Acknowledgement

The authors would like to thank Melexis for their technical, financial and logistical support in an IWT-funded project.

References

[1] S. Chatteriee, Y. Tsividis and P. Kinget, „0.5V analog circuit techniques and their application in OTA and filter design,“ Solid-state Circuits, IEEE Journal of, vol. 40, no. 12, pp. 2373–2387, 2005.

[2] G. C. M. Meijer, “Smart Sensor Systems,” Wiley, 2008.

[3] H. Danneels, F. Piette, G. Gielen, “A Novel PLL-based Sensor Interface for Resistive Pressure Sensors“, Proc. Eurosensors XXIV, September 2010.

[4] H. Danneels, F. Piette, V. De Smedt, W. Dehaene and G. Gielen, “A Novel, PLL-based Frequency-to-Digital Conversion Mechanism for Sensor Interfaces”, Sensors & Actuators: A. Physical (2011), available online.

[5] Sander L. J. Gierkink and Ed (A. J. M.) van Tuijl, A coupled Sawtooth Oscillator Combining Low Jitter With High Control Linearity, IEEE Journal of Solid-State Circuits, Vol. 37, NO. 6, June 2002.